8237-DMA Controller
Direct Memory Access

Figure 12.10
DMA Data Transfer

DMA Operation

✓ Direct Memory Access (DMA) is an I/O technique commonly used for high-speed data transfer; for example, data transfer between memory and a floppy disk.

✓ In DMA, μP releases the control of the buses to a device called a DMA controller. The controller manages data transfer between memory and a peripheral under its control, thus bypassing the MPU.

✓ It introduces two new signals **HOLD (pin 39)** and **HLDA (pin 38)** (Hold acknowledge)
✓ This is an active high input signal
✓ Pin number 39
✓ The processor relinquishes (gives up) the buses in the following machine cycle once the MPU receives the HOLD request
✓ All buses are tri-stated and HLDA (Hold Acknowledge) signal is sent out
✓ MPU regains the control of the buses after HOLD goes low
HLDA

✓ This is an active high output signal
✓ Pin number 38
✓ It indicates that the MPU is giving up the control of the buses
The DMA controller should have

I. A data bus
II. An address bus
III. Read/Write control signals, and
IV. Control signals to disable its role as a peripheral and to enable its role as a peripheral

(Note that DMA controller is a processor capable only of copying data at high speed from one location to another location)
8237 DMA CONTROLLER Block Diagram

FIGURE 15.33
8237A—DMA Controller with Internal Registers

- C$: Command Port
- Reg. Addr: Register Address
- Internal Registers:
  - 00: CH0 Memory Address Reg.
  - 01: CH0 Count Reg.
  - 02: CH1 Memory Address Reg.
  - 03: CH1 Count Reg.
  - 04: CH2 Memory Address Reg.
  - 05: CH2 Count Reg.
  - 06: CH3 Memory Address Reg.
  - 07: CH3 Count Reg.
  - 08: R/W Status/Command Reg.
  - 09: WR Request Reg.
  - 0A: WR Single Mask Reg.
  - 0B: WR Mode Reg.
  - 0C: WR Clear Byte Pointer F/F
  - 0D: R/W Master Clear/Toggle Reg.
  - 0E: WR Clear Mask Reg.
  - 0F: WR All Mask Reg. Bits

- DREQ0
- DREQ1
- DREQ2
- DREQ3
- DACK0
- DACK1
- DACK2
- DACK3
- EOF

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Features

✓ 8237 is a programmable Direct Memory Access controller (DMA) housed in a 40-pin package
✓ It has four independent channels with each channel capable of transferring 64K bytes
✓ It must interface with MPU and a peripheral device
✓ It is an I/O device to MPU
✓ It is a data transfer processor to peripheral device
✓ Many of its signals that are input in the I/O mode become outputs in the processor mode
Description

✓ The block diagram shows a logical pin out and internal registers of the 8237. It also shows the interface with the 8085 using a 3-to-8 decoder.

✓ 8237 has four independent channels CH0-CH3. Two 16-bit registers are internally associated with each channel.

✓ These registers are determined by A3-A0 and the chip select line (CS).

✓ The 8237 signals are divided into two groups:
  1) signals on left (used to communicate with MPU)
  2) signals on right (used to communicate with peripheral)

✓ Some of these signals are bidirectional and are determined by the DMA mode of operation (I/O or processor mode).
DMA Signals

✓ To obtain DMA service, a request is generated by activating the DREQ line of the channel.

✓ DACK are output lines to inform the individual peripherals that DMA is granted. DREQ and DACK are eqvt to handshake signals in I/O devices.

✓ AEN and ADSTB - Address Enable and Address Strobe are used to latch a high-order byte to generate a 16-bit address.

✓ After receiving the HRQ (Hold request), the MPU completes the bus cycle in process and issues the HLDA (Hold Acknowledgement) signal.
System Interface

✓ When a transfer begins, the DMA places the low-order byte on the address bus and high-order byte on the data bus

✓ Then 8237 asserts AEN (Address Enable) and ADSTB (Address Strobe)

✓ Theses two signals are used to latch the high-order byte from the data bus and 8237 places the 16-bit address on the system bus
FIGURE 15.34
Interfacing 8237A—DMA Controller with the 8085
NEXT CLASS

Serial Communication
(Chapter 16)
THANK YOU