8259-Programmable Interrupt Controller
(8259-PIC)
A Programmable interface device is designed to perform various input/output functions. Such a device can be set up to perform specific functions by writing an instruction (or instructions) in its internal register, called the control word.
Block Diagram

FIGURE 12.9
The 8259A Block Diagram

Features

The 8259 interrupt controller can:

- Manage eight interrupts according to the instructions written into its control registers. This is equivalent to providing eight interrupt pins on the processor in place of one INTR (8085) pin
- Vector an interrupt request anywhere in the memory map
- Resolve eight levels of interrupt priorities in a variety of modes, such as fully nested mode, automatic rotation mode, and specific rotation mode
- Mask each interrupt request individually
- Read the status of pending interrupts, in-service interrupts, and masked interrupts
- Be set up to accept either the level-triggered or the edge-triggered interrupt request
- Be expanded to 64 priority levels by cascading additional 8259s
- Be set up to work either with the 8085µP mode or the 8086/8088 µP mode
The internal block diagram of the 8259 includes eight block

I. Control Logic
II. Read/Write Logic
III. Data Bus Buffer
IV. Three Registers IRR, ISR, and IMR
V. Priority Resolver and
VI. Cascade Buffer
Read/Write Logic

When the address line A0 is at logic 0, the controller is selected to write a command or read a status.
Control Logic

- This block has two pins INT (interrupt) as an output, INTA (Interrupt Acknowledge) as an input.
- The INT is connected to the interrupt pin of the μP. Whenever a valid interrupt is asserted, this signal goes high. The INTA is the Interrupt Acknowledge signal from the μP.
The Interrupt Request Register (IRR) has eight input lines ($\text{IR}_0$-$\text{IR}_7$) for interrupts. When these lines go high, the requests are stored in the register.

The In-Service Register (ISR) stores all the levels that are currently being serviced, and the Interrupt Mask Register (IMR) stores the masking bits of the interrupt lines to be masked.

The Priority Resolver (PR) examines these three registers and determines whether INT should be sent to the \(\mu\)P.
Cascade Buffer/Comparator

✓ This block is used to expand the number of interrupt levels by cascading two or more 8259s
Interrupt Operation

To implement interrupts, the Interrupt Enable flip-flop in the μP should be enabled by writing the EI instruction, and the 8259 requires two types of control words; Initialization Command Words (ICWs) and Operational Command Words (OCWs)

**ICWs:**
ICWs are used to set up the proper conditions and specify RST vector addresses.

**OCWs:**
OCWs are used to perform functions such as masking interrupts, setting up status-read operations, etc.
After the initialization, the following sequence of events occurs when one or more interrupt request lines go high.

I. The IRR stores the requests
II. The priority resolver resolves the priority and sets the INT high when appropriate
III. The processor acknowledges the interrupt by sending INTA
IV. After the INTA is received, the appropriate priority bit in the ISR is set to indicate which interrupt level is being serviced, and the corresponding bit in the IRR is reset to indicate that the request is accepted. Then, the opcode for the CALL instruction is placed on the data bus
V. When the processor decodes the CALL instruction, it places two more INTA signals on the data bus
VI. When the 8259 receives the second INTA, it places the low order byte of the CALL address on the data bus. At the third INTA, it places the high-order byte on the data bus. CALL address is the vector memory location for the interrupt; this is placed in the control register during the initialization.
VII. During the 3rd INTA pulse, the ISR bit is reset
VIII. The program sequence is transferred to the memory location specified by the CALL
Programming the 8259

- The 8259 requires two types of command words, Initialization Command Words (ICWs) and Operational Command Words (OCWs).
- The 8259 can be initialized with four ICWs; the first two are essential, and the other two are optional based on the modes being used.
- These words must be issued in a given sequence.
- Once initialized, the 8259 can be set up to operate in various modes by using three different OCWs; however, they no longer need be issued in a specific sequence.

(Please see page 510 in text book for ICW1 and ICW2)
The ICW1 specifies:

- Single or multiple 8259s in the system
- 4-or 8-bit interval between the interrupt vector location
- The address bits $A_7$-$A_5$ of the CALL instructions; the rest are supplied by the 8259
FIGURE 15.30
Initialization Command Words for the 8259A

NEXT CLASS

8251
THANK YOU